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What Is Claimed Is:

1. An array substrate for in-plane switching mode liquid crystal display device, comprising:

a substrate having a plurality of pixel regions;

a plurality of gate lines and a plurality of common lines in horizontal direction;

a plurality of data lines crossing the gate line and the common line;

a thin film transistor at a cross point of the gate line and the data line, the thin film transistor having a gate electrode, an active layer, a source electrode and a drain electrode;

a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode to the pixel region, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and being connected to the vertical portion;

a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one portion; and

an auxiliary line over the horizontal portion of the pixel electrode and being overlapped with the common line.

2. The array substrate according to claim 1, further comprising a dummy line in a non-display area of the substrate.

3. The array substrate according to claim 2, wherein the dummy line communicates with the auxiliary line.

4. The array substrate according to claim 2, wherein the dummy line includes one of a metal material from the group of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

5. The array substrate according to claim 1, wherein the auxiliary line includes one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

6. The array substrate according to claim 1, wherein the gate line, the common line and the common electrode are formed using the same material on a same layer.

7. The array substrate according to claim 1, wherein the gate line, the common line and the common electrode includes one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

8. The array substrate according to claim 1, further comprising an insulating layer between the common line and the horizontal portion of the pixel electrode to form a first auxiliary storage capacitor.

9. The array substrate according to claim 8, wherein the insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

10. The array substrate according to claim 1, further comprising an insulating layer between the horizontal portion of the pixel electrode and the auxiliary line to form a second auxiliary storage capacitor.

11. The array substrate according to claim 10, wherein the insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

12. A method for fabricating an array substrate for in-plane switching mode liquid crystal display device, comprising:

forming a plurality of gate lines, a plurality of common lines and a dummy line on an array substrate, the gate line and the common line being formed in a horizontal direction and spaced apart from each other, the dummy line being formed in a non-display area;

forming a plurality of data lines crossing the gate line and the common line;

forming a thin film transistor at a cross point of the gate line and the data line, the thin film transistor having a gate electrode, an active layer, a source electrode and a drain electrode;

forming a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and connected to the vertical portion;

forming a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one portion; and

forming an auxiliary line over the horizontal portion of the pixel electrode, the auxiliary line being overlapped with the common line and one end of the auxiliary line communicating with the dummy line.

13. The method according to claim 12, wherein the gate line, the common line and the dummy line are formed using the same material on a same layer.

14. The method according to claim 12, wherein the gate line, the common line and the dummy line are formed one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

15. The method according to claim 12, wherein the auxiliary line is formed one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

16. The method according to claim 12, further comprising forming an insulating layer between the common line and the horizontal portion of the pixel electrode to form a first auxiliary storage capacitor.

17. The method according to claim 16, wherein the insulating layer is formed one of silicon nitride (SiNx) and silicon oxide (SiO_2).

18. The method according to claim 12, further comprising forming an insulating layer between the horizontal portion of the pixel electrode and the auxiliary line to form a second auxiliary storage capacitor.

19. The method according to claim 18, wherein the insulating layer is formed one of silicon nitride (SiNx) and silicon oxide (SiO_2).